IN THE CLAIMS:

Please amend claims 1, 2, 5, 9, 13, 17, 21, and 30 as follows:

1. (Currently Amended) A method ~~for controlling a cache,~~ comprising:

providing an instruction to ~~the~~ access valid data in a cache ~~indicating~~ and to indicate that a line storing the accessed valid data in the cache is a candidate for replacement by reducing an importance level of the line.

2. (Currently Amended) The method as recited in claim 1 further ~~comprising~~ comprising:

reducing an importance level of the line based on the instruction.

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3. (Previously Amended) The method as recited in claim 2 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

4. (Previously Amended) The method as recited in claim 3 wherein the replacement policy is a least recently used policy and wherein said other line is less recently used than the line.

5. (Currently Amended) The method as recited in claim 1 further ~~comprising~~ comprising:

altering an allocation methodology of the cache based on the instruction.

6. (Previously Amended) The method as recited in claim 1 wherein the instruction is part of an application kernel.

7. (Original) The method as recited in claim 1 wherein the instruction is generated by a compiler.

8. (Original) The method as recited in claim 1 wherein the instruction is an extension of a memory access instruction.

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9. (Currently Amended) An instruction for increasing hit rate of a cache, the instruction comprising a valid data memory access component and an indication that a line storing valid data in a memory of the cache is a candidate for replacement by reducing an importance level of the line.

10. (Original) The instruction as recited in claim 9 wherein the indication causes a reduction of an importance level of the line.

11. (Previously Amended) The instruction as recited in claim 10 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

12. (Previously Amended) The instruction as recited in claim 11 wherein the replacement policy is a least recently used policy and wherein said other line is less recently used than the line.

13. (Currently Amended) The instruction as recited in claim 9 further ~~comprising~~ comprising:

altering an allocation methodology of the cache based on the instruction.

14. (Original) The instruction as recited in claim 9 wherein the instruction in part of an application kernel.

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15. (Original) The instruction as recited in claim 9 wherein the instruction is generated by a compiler.

16. (Original) The instruction as recited in claim 9 wherein the instruction is an extension of a memory access instruction.

17. (Currently Amended) ~~An article comprising a storage medium, the storage medium having a set of instructions, the set of instructions being capable of being executed by at least one processor to implement a method for controlling a cache, the set of instructions when executed comprising~~ A machine-readable medium having stored thereon a plurality of executable instructions to perform a method comprising:

providing an instruction to access valid data in a cache and to indicate ~~indication to the cache~~ that a line storing the accessed valid data in the cache is a candidate for replacement by reducing an importance level of the line.

18. (Currently Amended) The article as recited in claim 17 wherein the set of instructions further ~~comprises~~ comprises:

reducing an importance level of the line based on the indication.

19. (Previously Amended) The article as recited in claim 18 wherein the reducing of the importance level of the line results in the line being replaced prior to an other line scheduled for replacement by a replacement policy of the cache.

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20. (Previously Amended) The article as recited in claim 19 wherein the replacement policy is a least recently used policy and wherein said other line is less recently used than the line.

21. (Currently Amendment) The article as recited in claim 17 further ~~comprising~~ comprising:

altering an allocation methodology of the cache based on the indication.

22. (Original) The article as recited in claim 17 wherein the indication is part of an application kernel.

23. (Original) The article as recited in claim 17 wherein the indication is generated by a compiler.

24. (Original) The article as recited in claim 17 wherein the indication is an extension of a memory access instruction.

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25. (Currently Amended) A cache comprising:

a cache memory including a cache line storing valid data; and

a cache control logic ~~for reducing~~ to receive an instruction to access the valid data and an indication to reduce an importance level of the cache line based on ~~an~~ the instruction.

26. (Original) The cache as recited in claim 25 wherein the instruction provides an indication that the cache line is a candidate for replacement.

27. (Original) The cache as recited in claim 26 wherein the cache control logic reduces an importance level of the cache line based on the indication.

28. (Original) The cache as recited in claim 27 wherein the reducing of the importance level of the cache line results in the cache line being replaced prior to another cache line scheduled for replacement by a replacement policy of the cache.

29. (Original) The cache as recited in claim 25 further comprising altering an allocation methodology of the cache based on the instruction.

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30. (Currently Amended) A method for controlling a cache, comprising:

providing an instruction to access valid data in the cache ~~indicating~~ and to indicate that a line storing the accessed valid data is a candidate for replacement by reducing an importance level of the line; and

reducing an importance level of the line based on the instruction.